

09/639197

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Class	Subclass
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ISSUE CLASSIFICATION

PA* ~~SECRET~~ VBER

U.S. UTILITY Patent Application

O.I.P.E.

PATENT DATE

SCANNED

BK③

 CS^2

APPLICATION NO.
09/639197

CONT/PRIOR

CLASS

SUBCLASS

ART UNIT 2310

EXAMINER

APPLICANTS

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Eamon Byrne
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Patrick Mitchell

TITLE

For an integrated approach to the design of digital converters, digital logic and high memory and an emulator

PTO-2040
12/99

ISSUING CLASSIFICATION

[illegible]☐ Continued on Issue Slip Inside File Jacket

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED		
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.	
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED		
				ISSUE FEE Amount Due Date Paid		
ISSUE BATCH NUMBER						
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____	_____ (Primary Examiner) (Date)					
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) (Date)					

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